UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/464,811	12/17/99	SHAO H	1-10-3

MM92/0517

DOCKET ADMINISTRATOR (RM 3C-512)
LUCENT TECHNOLOGIES INC
600 MOUNTAIN AVENUE
PO BOX 636
MURRAY HILL NJ 07974-0636

EXAMINER	
CRUZ,L	
ART UNIT	**PAPER NUMBER**
2815	2

DATE MAILED: 05/17/00

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No.	Applicant(s)	
	09/464,811	SHAO ET AL.	
	Examiner	Art Unit	
	Lourdes C. Cruz	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Status

1)☒ Responsive to communication(s) filed on *17 December 1999* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) *22-33* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claims *22-33* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 December 1999* is/are objected to by the Examiner.

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a)☐ All b)☐ Some * c)☐ None of the CERTIFIED copies of the priority documents have been:

1.☐ received.

2.☐ received in Application No. (Series Code / Serial Number) _____ .

3.☐ received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. & 119(e).

Attachment(s)

15) ☒ Notice of References Cited (PTO-892)
16) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
18) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
19) ☐ Notice of Informal Patent Application (PTO-152)
20) ☐ Other: .

DETAILED ACTION

This Office Action is in response to an Application filed December 17, 1999.

Election/Restrictions

Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-21, drawn to a semiconductor device, classified in class 257, subclass 758.

II. Claims 22-33, drawn to a method for making a semiconductor device, classified in class 438, subclass 1+.

The inventions are distinct, each from the other because of the following reasons:

Inventions I and II are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make other and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). In the instant case unpatentability of Group I invention does not necessarily imply unpatentability of Group II invention, since the device of Group I invention can be made by a materially different product than that disclosed in independent claim 22. For example, the device of Group I could be made by selectively depositing the second insulating layer, so that no etching is necessary after the depositing of the upper level of interconnect members over said second insulating layer.

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

During a telephone conversation with Mr. FERDINAND ROMANO on May 17, 200. a provisional election was made with traverse to prosecute the invention of Group I, claims1-21. Applicant in replying to this Office action must make affirmation of this election. Claims 22-33 withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a petition under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Drawings

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: For example, the drawings fail to show reference number 2500 (page 7 line 31), and reference number 350 (page 8, line 19) is not shown. Correction is required.

Applicant is required to submit a proposed drawing correction in reply to this Office action. However, formal correction of the noted defect can be deferred until the examiner allows the application.

Claim Objections

Claim 7 is objected to because of the following informalities: The claim's sole sentence has grammatical problems for it is missing a period to end the statement at the end of the sentence. Appropriate correction is required.

Claim 8 is objected to because of the following informalities: The claim has grammatical problems which make the claim unclear. See line 5 of the claim. Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 20 and 21 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

As to claim 20, refer to line 9 of the claim "said insulative material comprising a continuous layer extending from within regions between members of the upper level of interconnect to within regions between members of the lower level of interconnect"

Regarding claim 21, the recited structure is unclear as to enable one with ordinary skill in the art to clearly understand the claimed invention.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-21 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claims 1, and 11, the phrases "low dielectric constant " and "high dielectric constant" render the claims indefinite because adjectives such as "low" and "high" do not specifically describe a material or any property attributed to it, which in turn renders the scope of the claims unascertainable.

Claim 1 recites the limitation "the electronic device" in line 9. There is insufficient antecedent basis for this limitation in the claim.

Claim 5 recites the limitation "the lower insulative material"" in line 2. There is insufficient antecedent basis for this limitation in the claim.

Regarding claims 10, 20, and 21 the phrase "continuous" renders the claims indefinite because such phrase does not specifically describe how the layer extends from within regions of conductive members. It is unclear how such layer is continuous,

and what the applicant means by such terminology. The scope of the claims is thereby rendered indefinite by such limitation.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Jeng et al. (U.S. Patent No. 5818111).

Regarding claim 1, Jeng et al. disclose:

a semiconductor structure comprising a first upper level of interconnect members formed (See Fig. 3) over a semiconductor layer (10); at least one lower level of interconnect members formed between the semiconductor layer and the first upper level (See col. 4, lines 43+);

a first insulative material (18), having a relatively low dielectric constant (Col. 5, Table), positioned to electrically isolate members of the first upper level from one another and extending to the lower level of interconnect members; and

a second insulative material (22) having a relatively high dielectric constant (See Col. 5, Table), positioned to electrically isolate members of the lower level from some of the electronic devices (Col. 3, lines 53+).

With regard to claim 2, Jeng et al. disclose the semiconductor structure of claim 1 wherein a portion of the second insulative material (22) extends between an interconnect member of the lower level and an interconnect member of the upper level.

Regarding claim 3, Jeng et al. disclose the structure of claim 1 wherein the second insulative material (22) predominantly comprises silicon dioxide (Col. 5, Table) and the structure further includesa plurality of individual portions formed of the second insulative material, each portion extending between a member of the lower level and a member of the upper level and self-aligned with said member of the upper level.

Regarding claim 4, Jeng et al. disclose the structure of claim 1 including at least a second upper level of interconnect members formed over the first upper level (Col. 4, lines 43+).

Regarding claim 6, Jeng et al. disclose the structure of claim 1 wherein members of the first level (14) comprise Al,the first insulative material (18) comprises hydrogen silsesquioxane (Col. 5, Table) and the second insulative material (22) comprises silicon dioxide (Col. 5, Table).

Regarding claim 7, Jeng et al. disclose the structure of claim 1 further including a second upper level of interconnect members formed between the first upper level of interconnect members and the lower level of interconnect members (Col. 4, lines 43+) wherein potions of the lower insulative material electrically isolate the second upper level of interconnect members from the lower level of interconnect members.

Regarding claim 8, Jeng. et al. disclose the structure of claim 1 further including:

a plurality of additional upper levels of interconnect members formed between the first upper level and the lower level (Col. 4, lines 43+);

a first layer formed of the first insulative material (18) and positioned between the first upper level and a first of the additional levels (Col.4, lines 43+); and

a second layer formed of the first insulative material and positioned between second and third ones of the additional levels.

Regarding claim 9, Jeng et al. disclose the structure of claim 1 comprising second third, fourth and fifth upper levels of interconnect members formed between the first upper level and the lower level (Col. 4, lines 43+)

Regarding claim 10, Jeng et al. disclose the structure of claim 9 wherein the first, second, third, fourth and fifth upper levels are electrically isolated from one another by a continuous layer comprising the first insulative material (18).

Regarding claim 11, Jeng et al. disclose the structure of claim 9 wherein the first insulative material (18) is a single species of low k dielectric material (Col. 5, Table) and the second insulative material (22) predominantly comprises silicon dioxide (Col. 5, Table).

Regarding claim 12, Jeng et al. disclose the structure of claim 9 wherein multiple layers each comprising the first insulative material (18) electrically isolate the first, second, third, fourth and fifth upper levels from one another (Col. 4, lines 43+).

Regarding claim 13, Jeng et al. discloses the structure of claim 1 further including a second upper level of interconnect members formed between the first level of interconnect members and the lower level of interconnect members (14) wherein

portions of the second insulative material (22) extend to electrically isolate the second upper level of interconnect members from the lower level of interconnect members (See Fig. 3).

With regard to claim 14, Jeng et al disclose the structure of claim 12 wherein portions of the second insulative material (22) extend between two or more of the upper levels.

With regard to claim 15, Jeng et al. disclose the structure of claim 1 further including:

a first plurality of conductive portions (16) extending at least between the upper level of interconnect and the lower level of interconnect; and a second plurality of conductive portions (16) extending at least between the lower level of interconnect and some of the electronic devices (Col. 3, lines 53+)

With regard to claim 16, Jen et al. disclose the structure of claim 15 wherein the first plurality of conductive potrtions are integrally formed with members of the first upper level in (See Fig. 3) a dual Damascene structure in so much as "dual Damascene" structure denotes any specific structure or structural limitation.

Regarding claim 17, Jen et al. disclose the structure of claim 15 wherein all of the members (14) predominately comprise Al (See Fig. 3).

Regarding claim 18, Jeng et al. disclose the structure of claim 1 wherein the first insulative material extends from the first upper level to electrically isolate members of the lower level from one another (See Fig. 3).

Regarding claim 19, jeng et al. disclose the structure of claim 1 further including at least a second upper level of interconnect members (Col. 4, lines 43+) formed over the first upper level of interconnect members with the first insulative material (18) extending from the first upper level to electricallly isolate members (14) of the second upper level from one another.

With regard to claim 20, Jeng et al. disclose a semiconductor structure comprising:

A first upper level of interconnect members formed over a semiconductor layer (10); a lower level of interconnect members (14) formed between the semiconductor layer and the first upper level (Col. 4, lines 43+); and insulative (18) positiones to electrically isolate portions of the upper level of interconnect members (14) from one another, portions of the upper level of interconnect members (14) from portions of the lower level of interconnect members and portions of the lower level of interconnect members (14) from one another,

Said insulative material (18) comprising a continuous layer extending from within regions between members of the upper level of interconnect to within regions between members of the lower level of interconnect (See Fig. 3) said continuous layer characterized by a dielectric constant of less than 3.9 (Col. 5, Table).

Also regarding claims 1,5, and 20, see In re Pearson 181 USPQ 641 (CCPA) which makes clear that terms merely setting forth intended use for, or a property inherent in, an otherwise old composition do not differentiate claimed composition from those known to prior art. See also, In re Swinehart [169 USPQ 226] (CCPA 1971)

which makes clear that mere recitation of a newly discovered function or property, inherently possessed by things in prior art, does not cause claim drawn to those things to distinguish over prior art.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Jeng (U.S. Patent No. 6054769) discloses a low capacitance interconnect structure. Jeng (U.S. Patent No. 5858871) discloses a porous insulator for capacitance reduction. Chen et al. (U.S. Patent No. 5976984) disclose a process of making unlanded vias. Jeng (U.S. Patent No. 5548159) discloses a line to line capacitance reduction insulator. Dawson et al. (U.S. Patent No. 5783864) disclose a multtilayer interconnect structure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lourdes C. Cruz whose telephone number is 707-306-5691. The examiner can normally be reached on M-F 8:00- 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mahshid D Saadat can be reached on 703-308-0956. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Lourdes C. Cruz
Examiner
Art Unit 2815

Lourdes Cruz
May 12, 2000

DAVID HARDY
PRIMARY EXAMINER